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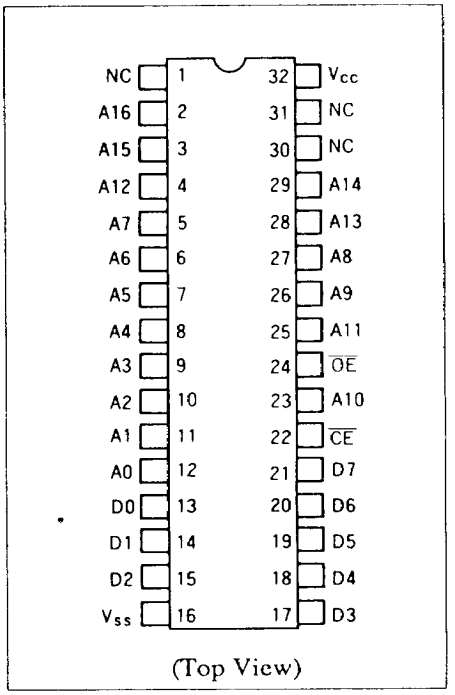
AKN62321A Series
AKN62331A Series

131072-Word × 8-Bit CMOS Mask Programmable ROM

PIN CONFIGURATION



(Top View)

AKN62321A, AKN62331A Series is a 1-Mbit CMOS mask-programable ROM organized to 131072-word x 8-bit. It can be operated with a battery because of low power consumption. The large capacity of 1M bits is optimum for a kanji character generator.

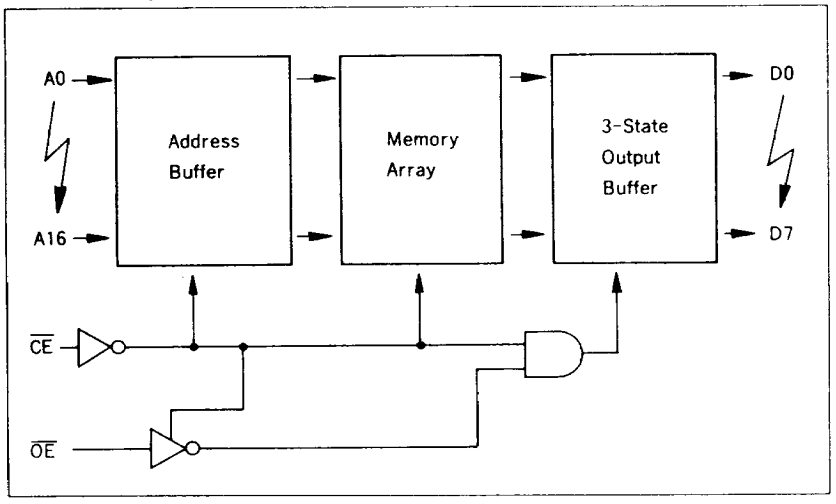
Features

- Single 5 V
- Wired OR is permitted for the output in three states
- TTL compatible
- Address access time: 120/150 ns (max)
- Low power: Active 100 mW (typ)
  Standby 5 µW (typ)
- Byte-Wide Data Organization, JEDEC pin arrangement

Ordering Information

Type No.	Address Access Time	Package
AKN62321AP	150 ns	600 mil 32-pin
AKN62331AP	120 ns	plastic DIP
AKN62321AF	150 ns	32-pin
AKN62331AF	120 ns	plastic SOP

Block Diagram



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Absolute Maximum Ratings

Item	Symbol	Rating	Unit
Power supply voltage*1	Vcc	–0.3 to +7.0	V
Terminal voltage*1	VT	–0.3 to Vcc + 0.3	V
Operating temperature	Topr	0 to +70	°C
Storage temperature	Tstg	–55 to +125	°C
Bias temperature	Tbias	–20 to +85	°C

Note: *1. With respect to Vss.

Recommended Operating Conditions (Vss = 0 V, Ta = 0 to +70°C)

Item	Symbol	Min	Typ	Max	Unit
Power supply voltage	Vcc	4.5	5.0	5.5	V
Input voltage	VIH	2.2	—	Vcc + 0.3	V
	VIL	–0.3	—	0.8	V

DC Characteristics (Vcc = 5 V ± 10%, Vss = 0 V, Ta = 0 to +70°C)

Item		Symbol	Min	Max	Unit	Test Conditions
Power supply current	Active	Icc	—	50	mA	Vcc = 5.5 V, IDOUT = 0 mA, tRC = Min
	Standby	ISB	—	30	µA	Vcc = 5.5 V, $\overline{CE}$ ≥ Vcc –0.2 V
Input leak current		| ILI |	—	10	µA	VIN = 0 to Vcc
Output leak current		| ILO |	—	10	µA	$\overline{CE}$ = 2.2 V, VOUT = 0 to Vcc
Output voltage		VOH	2.4	—	V	IOH = –205 µA
		VOL	—	0.4	V	IOL = 3.2 mA

Capacitance (Vcc = 5 V ± 10%, Vss = 0 V, Ta = 25°C, Vin = 0 V, f = 1 MHz)

Item	Symbol	Min	Max	Unit
Input capacitance*1	Cin	—	10	pF
Output capacitance*1	Cout	—	15	pF

Note: *1. This parameter is sampled and not 100% tested.

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AC Operating Characteristics (V_{CC} = 5 V ± 10%, V_{SS} = 0 V, Ta = 0 to +70°C)

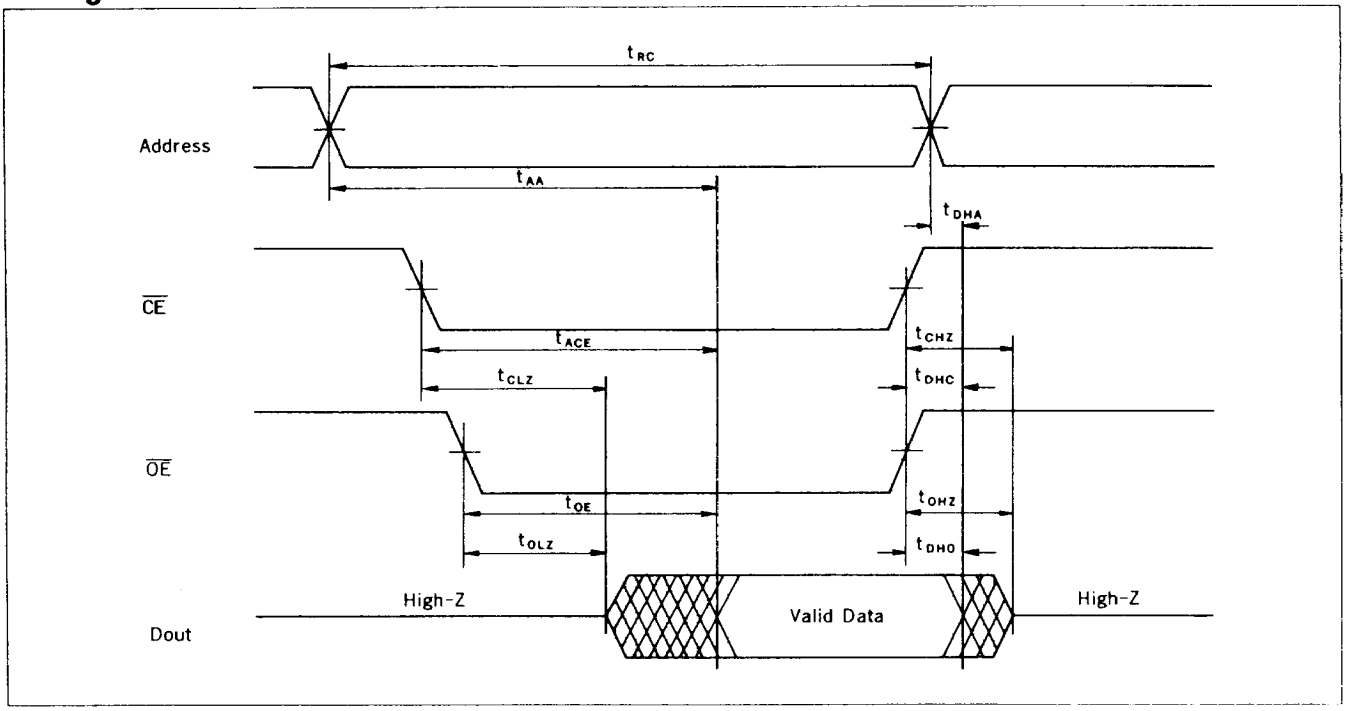
Test Conditions

Input pulse level: 0.8 to 2.4 V
I/O timing reference level: 1.5 V
Input rise/fall time: 10 ns
Output load: 1 TTL gate + C_L = 100 pF (including jig capacitance)

Item	Symbol	AKN62331A		AKN62321A		Unit
		Min	Max	Min	Max	
Cycle time	t_{RC}	120	—	150	—	ns
Address access time	t_{AA}	—	120	—	150	ns
$\overline{CE}$ access time	t_{ACE}	—	120	—	150	ns
$\overline{OE}$ access time	t_{OE}	—	60	—	70	ns
Output Hold Time from Address Change	t_{DHA}	0	—	0	—	ns
Output Hold Time from $\overline{CE}$	t_{DHC}	0	—	0	—	ns
Output Hold Time from $\overline{OE}$	t_{DHO}	0	—	0	—	ns
$\overline{CE}$ to Input in High Z	t_{CHZ}*1	—	60	—	70	ns
$\overline{OE}$ to Input in High Z	t_{OHZ}*1	—	60	—	70	ns
$\overline{CE}$ to Output in Low Z	t_{CLZ}	5	—	10	—	ns
$\overline{OE}$ to Output in Low Z	t_{OLZ}	5	–	10	–	ns

Note: *1. t_{CHZ} and t_{OHZ} define the time at which the output goes to the high impedance state and is not referenced to output voltage levels.

Timing Waveform



Notes: 1. t_{DHA}, t_{DHC}, t_{DHO}; Determined by whichever is faster.
2. t_{AA}, t_{ACE}, t_{OE}; Determined by whichever is slower.
3. t_{CLZ}, t_{OLZ}; Determined by whichever is slower.

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